UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/689,506 | 10/20/2003 | Huajie Chen | FIS920030241US1 | 4303 |

7590 04/11/2006

Andrew M. Calderon
Greenblum and Bernstein P.L.C.
1950 Roland Clarke Place
Reston, VA 20191

| EXAMINER | |
|---|---|
| MITCHELL, JAMES M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/689,506 | CHEN ET AL. | |
| | Examiner | Art Unit | |
| | James M. Mitchell | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to applicant's remarks filed December 1, 2005. The indicated allowability of claims 5 and 13 are withdrawn in view of the newly discovered references. Rejections based on the newly cited reference(s) follow.

### *Response to Amendment*

The Declaration filed on December 1, 2005 under 37 CFR 1.131 is sufficient to overcome the Ouyang (U.S. 2004/0256814) reference.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 8-12, 14,16 and 17are rejected under 35 U.S.C. 102(e) as being anticipated by Baba et al. (U.S. 6,774,409).

Baba (Fig. 2-5) discloses:

(cl. 1) a method of manufacturing a semiconductor structure, comprising the steps of: forming a p-type field-effect-transistor (pFET) channel (57) and a n-type field-effect- transistor (nFET) channel (57) in a substrate, forming a PFET stack in the

PFET channel and an nFET stack in the nFET channel, providing a first layer ("SiGe"; e.g. 42; Title) of material at source/drain regions (e.g. channel located near and therefore at region of source) associated with the PFET stack, the first layer (4) of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state (Col. 4, Lines 58) within the PFET channel, and providing a second layer (5) of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state[1] at the nFET channel;

(cl. 2, 11) the first layer of material is SiGe having a content of Ge approximately greater than 0% in ratio to Si (Col. 4, Lines 9-10);

(cl. 3) the second layer of material is Si:C (e.g. Title of Baba);

(cl. 4) wherein the Si:C has a content of C of about 4% or less (Col. 4, Lines 18-21)

(cl. 8, 16) the first layer of material and the second layer of material are each grown(col. 4, Lines 48-50) to a thickness about 10 to 100 nm (Col. 4, Lines 9-11 & 20-22);

(cl. 9, 14) the first and the second layer of material are embedded in the layer (e.g. in item 2, 3; Fig. 1d);

(cl. 10) a method of manufacturing a semiconductor structure, comprising the steps of: forming a p-type field-effect-transistor (pFET) channel (57) and a n-type field-effect- transistor (nFET) channel (57) in a substrate, forming a PFET stack in the PFET channel and an nFET stack in the nFET channel, providing a first layer ("SiGe"; e.g. 42; Title) of material at source/drain regions (e.g. channel located near and

[1] Si:C same material as claimed by applicant, which results in same effects. See applicant's claim 3.

therefore at region of source) associated with the PFET stack, the first layer (4) of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state (Col. 4, Lines 58) within the PFET channel, and providing a second layer (5) of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel; and doping (Col. 4, Lines 28-29) source and drain regions of the nFET and pFET structures;

(cl. 12) a first material creates a compressive state (Col. 4, Lines 58) and a second material create a tensile state[2] ;

(cl. 17) an unrelaxed SIGe (e.g. forming compressive state ;Col. 4, Lines 58).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-6, 8, 10-13 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ka et al. (U.S. 2005/0035470) in combination with Murthy et al. (U.S. 2003/0080361).

Ka (Fig. 3g) discloses:

(cl. 1, 10) a method of manufacturing a semiconductor structure, comprising

[2] Si:C same material as claimed by applicant, which results in same effects. See applicant's claim 3.

the steps of: forming a p-type field-effect-transistor (pFET) channel (200) and a n-type field-effect- transistor (nFET) channel (201) in a substrate (202), forming a PFET stack in the PFET channel and an nFET stack in the nFET channel (Par. 0042), providing a first layer (238) of material at source/drain regions (e.g. channel located near and therefore at region of source) associated with the PFET stack, the first layer ("high strain) of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state (Par. 0043) within the PFET channel, and providing a second layer (228) of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state (Par. 0042) at the nFET channel;

(cont. cl. 10, cl. 18) and doping (CLM 86 of Ka) source and drain regions of the nFET and pFET structures;

(cl. 6, 13) placing a mask and etching regions (e.g. 220) of FET and selectively growing first and second material (Fig. 4a-b; Par. 0046);

(cl. 15) wherein the first material and second material are raised above a surface of the substrate (Fig. 3g).

Ka discloses that its high stress/unrelaxed layer (228,238) may be any other high stress film/material (Par. 0038), but does not explicitly disclose that the material is high stress/unrelaxed SiGe or Si:C.

Murthy utilizes high stress/unrelaxed film[3] SiGe and Si:C (Par. 0025, 0029).

[3] Changing channels to either tensile or compressively strained.

It would have been obvious to one of ordinary skill in the art to form the high stress films of Ka of SiGe and Si:C in order to provide tensile and compressive stress/strain as taught by Murthy (Par. 0025, 0029) and required by Ka (Par. 0042, 0043).

With respect to the ratio of Ge or C in Silicon of claims 2, 4, the prior art discloses the claimed invention except for the percentages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to change the percentage, since it has been held that where the general working conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

With respect to the claimed thickness of claim 5, 8, 16, applicant has not disclosed that the claimed thickness is for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the claimed thickness would have been obvious, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

***Allowable Subject Matter***

Claims 7are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or make obvious use of a protective sheet under a mask including all the limitations of the independent claims.

### *Response to Arguments*

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses the use of forming layers to induce strain on FET.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
April 7, 2006

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800